REMARKS

Claim 20 has been rewritten in independent form and is the same claim as was originally presented.

The Examiner rejected claims 1-5 and 8-11 under 35 U.S.C. §102(b) as allegedly being anticipated by US Pat. 5811211 to Tanaka et al.

The Examiner rejected claims 6, 7, and 12-20 under 35 U.S.C. §103(a) as allegedly being unpatentable over Tanaka in view of US Pat. 5376482 to Hwang et al.

Applicants respectfully traverse the §102(b) and §103(a) rejections with the following arguments.

35 U.S.C. §102(b)

The Examiner rejected claims 1-5 and 8-11 under 35 U.S.C. §102(b) as allegedly being anticipated by US Pat. 5811211 to Tanaka et al.

Applicants respectfully contend that Tanaka does not anticipate claims 1 and 8, because Tanaka does not teach each and every feature of claims 1 and 8.

For example with respect to claim 1, Tanaka does not teach the feature: "printing a design only within a peripheral portion of the wafer such that no portion of the printed design is within the active portion of the wafer, wherein the peripheral portion of the wafer is between an outer boundary of the active portion of the wafer and an outer boundary of the wafer".

With respect to claim 8, Tanaka does not teach the similar feature: "an image of a portion of the pattern is printed as a design only within a peripheral portion of the wafer such that no portion of the printed design is within the active portion of the wafer, wherein the peripheral portion of the wafer is between an outer boundary of the active portion of the wafer and an outer boundary of the wafer".

Thus, claims 1 and 8 each recite printing a design between an outer boundary of the active portion of the wafer and an outer boundary of the wafer.

Tanaka does not teach printing a design only between an outer boundary of the active portion of the wafer and an outer boundary of the wafer such that no portion of the printed design is within the active portion of the wafer, as required by claims 1 and 8. Indeed, Tanaka does not define the peripheral portion of the wafer (in which a design is printed) as being between an outer boundary of the active portion of the wafer and an outer boundary of the wafer. In fact, Tanaka provides no definition of the peripheral portion of the wafer and most certainly does not state any

geometrical relationship between a peripheral region and an active region of a wafer. In essence, Tanaka is totally ambiguous as to what the peripheral portion of the wafer actually means relative to the active portion of the wafer and most certainly does not teach that no portion of the printed design is within the active portion of the wafer. Therefore, Tanaka not teach the aforementioned features of claims 1 and 8.

Based on the preceding arguments, Applicants respectfully maintain that Tanaka does not anticipate claims 1 and 8, and that claims 1 and 8 are in condition for allowance. Since claims 2-5 depend from claim 1, Applicants contend that claims 2-5 are likewise in condition for allowance. Since claims 9-11 depend from claim 8, Applicants contend that claims 9-11 are likewise in condition for allowance.

In addition, the dependent claims have additional features not taught by Tanaka. For example with respect to claims and 10, Tanaka does not teach the feature: "wherein the spacing is about equal to a design tolerance, wherein the design tolerance is a sum of a first design tolerance and a second design tolerance, wherein the first design tolerance is based on how accurately the reticle blind can be positioned within the exposure apparatus, and wherein the second design tolerance is based on how sharply an edge of the reticle blind can be focused on the wafer by a lens of the exposure apparatus".

The Examiner argues: "Tanaka teaches a scale pattern (fig.5) that measures [cl.5,11] the accuracy of the blind settings (6;38-45) comprising numerical patterns (14;6-15) separated from the scale pattern [cl.3,9]. Tanaka teaches that the reticle graduations measure real distances printed on the wafer (14;16-23) and are used to determine the settings of the reticle blind

(14;24-45). The accuracy of the image printed on the wafer is the sum of all the errors (design tolerances) as shown in fig. 10; this is known in the art as the error budget. Tanaka teaches (14;16-23&17;58-18;14) that the graduations on the scale are designed to measure the minimum error expected from the error budget [cl.4,10]."

In response, Applicants contend that the Examiner's argument has not cited anything in Tanaka which teaches that a spacing between adjacent pattern elements is a sum of the first and second design tolerances recited in the preceding feature of claims 4 and 10. Therefore, claims 4 and 10 are not anticipated by Tanaka.

35 U.S.C. §103(a)

The Examiner rejected claims 6-7 and 12-20 under 35 U.S.C. §103(a) as allegedly being unpatentable over Tanaka in view of US Pat. 5376482 to Hwang et al.

As to claim 20, the Examiner has not presented any argument at all to support the rejection of claim 20 and therefore has not established a *prima facie* case of obviousness in relation to claim 20. Accordingly, Applicants respectfully request that the Examiner either present an argument to support the rejection of claim 20 or else indicate that claim 20 is allowed.

Since claims 6-7 depend from claim 1, which Applicants have argued *supra* to be patentable over Tanaka under 35 U.S.C. §102, Applicants maintain that claims 6-7 are not unpatentable over Tanaka in view of Hwang under 35 U.S.C. §103(a).

Since claim 12 depends from claim 8, which Applicants have argued *supra* to be patentable over Tanaka under 35 U.S.C. §102, Applicants maintain that claim 12 is not unpatentable over Tanaka in view of Hwang under 35 U.S.C. §103(a).

In addition, Applicants respectfully contend that claims 6-7 and 13 are not unpatentable over Tanaka in view Hwang, because Tanaka in view of Hwang does not teach or suggest each and every feature of claims 6-7 and 13. For example, Tanaka in view of Hwang does not teach or suggest the feature: "wherein the remaining portion of the light prints a device field within the active portion of the wafer, and wherein the device field and the design are each adjacent to a same portion of the outer boundary of the active portion of the wafer".

In relation to claims 6-7 and 12, the Examiner admits that Tanaka "does not explicitly teach patterning the active area and the peripheral area". Applicants argue that Hwang likewise does not disclose patterning the active area and the peripheral area. Applicants note that the Examiner does not allege that Hwang discloses patterning the active area and the peripheral area. Since neither Tanaka nor Hwang disclose the preceding feature of claims 6-7 and 12, Applicants respectfully contend that the Examiner has not established a *prima facie* case of obviousness in relation to claims 6-7 and 12. It is well established by law that the references cited to support the rejection of a claim under 35 U.S.C. §103(a) must teach or suggest every feature of the claim.

As to claims 13-15, the Examiner does not appear to have presented arguments directed specifically to claims 13-15. In any event, Applicants respectfully contend that claims 13-15, as well as claims 16-19, recite the following feature not taught or suggested by Tanaka in view of Hwang: "a design printed only within a peripheral portion of the wafer such that no portion of the printed design is within the active portion of the wafer, wherein the peripheral portion of the wafer is between an outer boundary of the active portion of the wafer and an outer boundary of the wafer". As explained *supra* by Applicants in relation to claims 1 and 8, Tanaka does not disclose the preceding feature of claims 13-19. In addition, Hwang does not disclose the preceding feature of claims 13-19. Since neither Tanaka nor Hwang disclose the preceding feature of claims 13-19, Applicants respectfully contend that the Examiner has not established a *prima facie* case of obviousness in relation to claims 13-19.

In addition with respect to claim 17, Applicants refer to Applicants' arguments *supra* in relation to claims 4 and 10.

Based on the preceding arguments, Applicants respectfully maintain that claims 6-7 and 12-20 are not unpatentable over Tanaka in view of Hwang, and that claims 6-7 and 12-20 are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account No. 09-0456.

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